

Applicant(s)	James D. Beasom	INFORMATION DISCLOSURE STATEMENT
Serial No.	Unknown	
Filing Date	Herewith	
Group Art Unit	Unknown	
Examiner	Unknown	
Attorney Docket No.	125.008US02	
Title: INTEGRATED CIRCUIT WITH A MOS STRUCTURE HAVING REDUCED PARASITIC BIPOLAR TRANSISTOR ACTION		

Mail Stop Patent Application
 Commissioner for Patents
 P.O. Box 1450
 Alexandria, VA 22313-1450

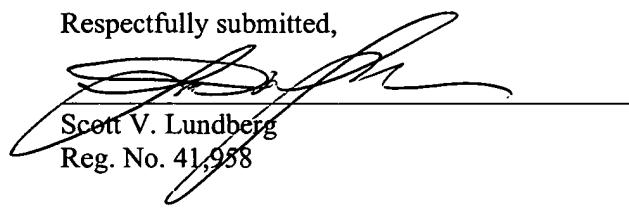
In compliance with 37 C.F.R. §§ 1.56 and 1.97, *et seq.*, the enclosed materials are brought to the attention of the Examiner for consideration in connection with the above-identified Application. Applicant respectfully requests that this Information Disclosure Statement be entered and the references listed on the attached Form 1449 be considered by the Examiner and made of record. Pursuant to MPEP §609, Applicant further requests that the Examiner initial next to each reference on the Form 1449 to indicate that the listed references have been considered. Applicant further requests that a copy of the initialed Form 1449 be returned with the next official communication.

Further pursuant to MPEP §609, because all of the references listed on the attached Form 1449 have been previously submitted and made of record in the parent application, U.S. Patent Application 09/977,188, filed October 12, 2001, copies of the references previously made of record in the parent application are not submitted herewith.

The Examiner is invited to contact the Applicant's Representative at the below-listed telephone number if there are any questions regarding this communication.

Respectfully submitted,

Date: 3-26-04


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Examiner Name	Unassigned	
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Title: INTEGRATED CIRCUIT WITH A MOS STRUCTURE HAVING REDUCED PARASITIC BIPOLAR TRANSISTOR ACTION

Sheet 1 of 1

U.S. Patent References				
Examiner Initials	Patent No.	Issue Date	Name	Filing Date
	4,564,770	01/14/86	Sherman et al.	03/29/83
	4,969,852	11/13/90	Osterwald	09/13/89
	5,138,177	08/11/92	Morgan et al.	03/26/91
	5,698,867	12/16/97	Bauer et al.	03/24/95
	5,821,144	10/13/98	D'Anna et al.	09/29/97
	6,035,235	03/07/00	Perttu et al.	03/30/98
	6,133,107	10/17/00	Menegoli	03/03/99
	6,166,925	12/26/00	Richter et al.	08/06/99
	6,172,398	01/09/01	Hshieh	08/11/97
	6,239,958	05/29/01	Kato et al.	12/18/98
	6,368,920	04/09/02	Beasom	06/11/98

Foreign Patent References				
Examiner Initials	Foreign Patent		Name	Publication Date
	Country	No.		
	EP	0747958		12/11/1996
	JP	7-193231		09/25/2001
	EP	0747966		11/12/1996
	WO	00/10204		02/24/2000
	JP	63281468		11/1998

Other References				
Examiner Initials	Author, Title, Date, Pages, etc.			
	Mizuno et al., Publication No: US 2001/0048119, "Semiconductor Device and Method of Manufacturing The Same", Published 12/06/01, Filed March 19, 2001.			
	Blanchard et al., Publication No. US 2002/0017684, "Transistor with Integrated Photodetector for Conductivity Modulation", Published 02/14/02, Filed 04/27/00.			

Examiner Signature		Date Considered	
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*Examiner: Initial if citation considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.